

ENGINEERING

DataXpress

DXL892-10 Advanced Mentor V8 to Composer Schematic Translator

The DXL892-10 Advanced Mentor V8 to Cadence Composer schematic translator is one of a series of optimized data links that is part of the DataXpress Integrator™ product line. The DataXpress Integrator was developed as a solution to the problem of moving design data from one EDA vendor's tools to another's.

The DXL892-10 translates Mentor Graphics Design Architect schematics to the Cadence Composer schematic system. It includes advanced features which support the translation of Mentor Frames and "parameterized hierarchy".

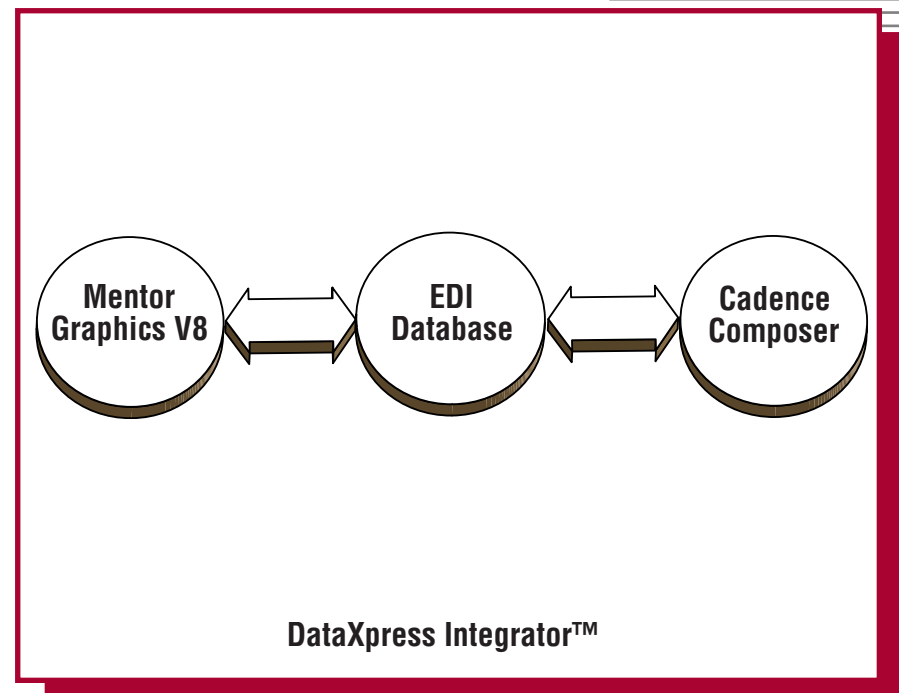
Schematics and cell libraries can be transferred independently, or a schematic and its library of subcomponents can be transferred at the same time. The full design hierarchy can be transferred or it can be limited in various ways. Options and commands for the translator are specified on the command line or in a configuration file.

Mentor "IF", "FOR", and "CASE" frames are translated. Any valid frame expression is handled by the translator, including those that are a function of one or more parameter variables. Also, "parameterized hierarchy" (design hierarchy that is a function of parameter values) is handled so that parameterized designs can be represented in the Cadence Composer schematic system.

The DXL892-10 Schematic Translator is fully supported by Engineering DataXpress, a worldwide leader in data translation technology. This support ensures that the translator will continue to be enhanced with new features and options and will remain current with each new release of Mentor Graphics software.

Features

- Translation of Mentor Graphics Design Architect sheets and symbols.
- Can translate frames, connectivity by name, busses, and comment graphics.
- Handles parameterized designs.
- User control over name mapping, grids, library transfer, etc.
- Handles hierarchy represented by Mentor Graphics sheets, symbols, and libraries.



Product Description

The DXL892-10 schematic translator transfers schematic and symbol information out of Mentor Graphics Design Architect to the DataXpress EDI database. The design is then analyzed for parameterized information and frames. If such design information is present, the DXL892-10 converts it so that it is compatible with the Cadence Composer schematic system. The design is then further translated from the EDI database to the Cadence Composer schematic system.

The DXL892-10 translator is comprised of two modules. The mda2edi module takes as its input schematics and symbols created with Design Architect and creates as its output either an EDI database or an EDIF file describing the schematics and/or symbols. The fed2cad module takes an EDIF input file or EDI database, processes any Mentor Frame or Parameterized information so that it can be represented by Cadence Composer, and then creates Cadence Composer schematics and/or symbols which can then be edited with Composer. The reader can also read and translate any correct EDIF level 0 schematic representation into Cadence Composer.

Mentor Graphics specific elements such as connectivity by name, both between sheets and to members of busses, rippers, off-page connectors, net connectors, and graphics are all translated to the equivalent Cadence Composer representations. Mentor Graphics "frames" are written into the EDI database, or optionally to an EDIF file, such that they can be extracted as frames by another system which is capable of handling frames. For systems that do not support frames, the frame is read as comment graphics.

The translator uses commands from the command line and/or configuration files to determine user options and to locate files in a design hierarchy. Using a configuration file, the user can specify globally for the entire translation or within a specific library or cell how various properties and attributes are to be mapped to Cadence Composer.

By default, a complete design hierarchy is translated. Simple commands limit the traversal of the hierarchy to only those schematics and symbols which are to be translated.

Using configuration files and/or command line options, the user can specify the following to control the translation process:

- Which schematics, symbols and cell libraries to translate.
- Scaling of sheets and symbols.
- Name mapping by character, substring, prefix and suffix for nets, symbols, instances and properties.
- How properties map.
- The value of global parameters.
- Translation of cell libraries.
- Translation of design hierarchy.
- Overwriting of schematics and symbols.

Supported Platforms

- Sun4/SunOS 4.1.4+.
- Sun4/SunOS 5.x (Solaris 2.x).
- HP 9000/7xx HP-UX 9.xx or greater.

Software Requirements

- Design Architect software Release 8.x or later.
- Cadence Composer software Release 4.2 or greater.
- EDIF version 2 0 0.

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